Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-31. (Cancelled)

Claim 32 (Currently amended). A semiconductor component comprising:

at least two electrodes; and

a semiconductor body coupled to the at least two electrodes, the semiconductor body including at least one pn junction and a voltage taking-up region of a first conduction type in which a space charge zone propagates if a voltage that reverse-biases the pn junction is applied to the electrodes,

wherein the voltage taking-up region further includes a temporarily effective area of the first conduction type having, between a conduction band and a valence band, centers configured to trap free charge carriers in the event of flooding of the voltage taking-up region, and to discharge the charge carriers in the event of propagation of the space charge zone, such that the area is temporarily effective corresponding to the event of a turn-off operation after flooding with free charge carriers, wherein the temporarily effective area is arranged at a depth of substantially between 0.75 W_B to 0.95 W_B from the pn junction, where W_B denotes the distance between the pn junction and an opposite edge of the voltage taking-up region.

Claim 33 (Previously presented). The semiconductor component as claimed in claim 32, further comprising a zone doped more highly than the voltage taking-up region disposed

between said voltage taking-up region and a first of the two electrodes, and wherein the temporarily effective area is arranged in the voltage taking-up region.

Claim 34 (Previously presented). The semiconductor component as claimed in claim 33, wherein the more highly doped zone has the first conduction type.

Claim 35 (Previously presented). The semiconductor component as claimed in claim 1, wherein the more highly doped zone has a second conduction type opposite to the first conduction type.

Claim 36 (Previously presented). The semiconductor component as claimed in claim 1, wherein the first conduction type is the n conduction type.

Claim 37 (Previously presented). The semiconductor component as claimed in one of claims 1, wherein the centers comprise K centers.

Claim 38 (Previously presented). The semiconductor component as claimed in claim 37, wherein the K centers comprise the association of a carbon atom, an oxygen atom and two vacancies (COVV).

Claim 39 (Previously presented). The semiconductor component as claimed in claim 37, wherein the K centers are produced by irradiation with high-energy particles.

Claim 40 (Previously presented). The semiconductor component as claimed in claim 39, wherein the K centers have a relative concentration corresponding to being produced by annealing at a temperature of more than 300°C subsequent to the irradiation.

Claim 41 (Previously presented). The semiconductor component as claimed in claim 39, wherein the high-energy particles comprise protons or helium nuclei.

Claim 42 (Previously presented). The semiconductor component as claimed in claim 39, wherein the high-energy particles comprise carbon atoms which form K centers and contribute to the material of the semiconductor body.

Claim 43 (Previously presented). The semiconductor component as claimed in claim 32, wherein the temporarily effective area comprises a field stopping area.

Claim 44 (Previously presented). The semiconductor component as claimed in claim 32, wherein the temporarily effective area has a doping concentration of substantially between 1 E 14 cm^{-3} and 5 E 15 cm^{-3}.

Claim 45 (Previously presented). The semiconductor component as claimed in claim 44, wherein the doping concentration is substantially between 1 E 14 cm^{-3} and 2 E 15 cm^{-3}.

Claim 46 (Previously presented). The semiconductor component as claimed in claim 32, wherein the pn junction forms a part of one of a group consisting of a diode, IGBT, thyristor or MOSFET.

Claim 47 (Previously presented). The semiconductor component as claimed in claim 46, wherein the voltage taking-up region further includes compensation regions of a second conduction type.

Claim 48 (Previously presented). The semiconductor component as claimed in claim 32, further comprising a steady-state field stopping area.

Claim 49 (Previously presented). The semiconductor component as claimed in claim 32, further comprising at least one further temporarily effective area in addition to the temporarily effective area.

Claim 50 (Previously presented). The semiconductor component as claimed in claim 49, wherein the temporarily effective area and the at least one further tempoerarily effective area are produced by multiple implantations.

Claim 51 (Previously presented). The semiconductor component as claimed in claims 32, wherein the semiconductor body is structured vertically.

Claim 52 (Previously presented). The semiconductor component as claimed in claim 32, wherein the semiconductor body is structured laterally.

Claim 53 (Currently amended). A method for production of the semiconductor component comprising at least two electrodes and a semiconductor body coupled to the at least two electrodes and a semiconductor body coupled to the at least two electrodes, the semiconductor

body including at least one pn junction and a voltage taking-up region of a first conduction type in which a space charge zone propagates if a voltage that reverse-biases the pn junction is applied to the electrodes,

wherein the voltage taking-up region further includes a temporarily effective area of the first conduction type having, between a conduction band and a valence band, centers configured to trap free charge carriers in the event of flooding of the voltage taking-up region, and to discharge the charge carriers in the event of propagation of the space charge zone, such that the area is temporarily effective corresponding to the event of a turn-off operation after flooding with free charge carriers, wherein the temporarily effective area is arranged at a depth of substantially between 0.75 W_B to 0.95 W_B from the pn junction, where W_B denotes the distance between the pn junction and an opposite edge of the voltage taking-up region, the method comprising:

introducing K centers by implantation of high-energy particles into a weakly doped region of the semiconductor body.

Claim 54 (Previously presented). The method as claimed in claim 53, further comprising performing annealing at a temperature of more than 300°C subsequent to the irradiation.

Claim 55 (Previously presented). The method as claimed in claim 53, wherein the high-energy particles comprise protons or helium nuclei.

Claim 56 (Previously presented). The method as claimed in claim 53, wherein the high-energy particles comprise carbon atoms.

Claim 57 (Previously presented). The method as claimed in claim 54, wherein the annealing is performed at a temperature of more than 420°C.

Claim 58 (Previously presented). The method as claimed in claim 53, further comprising performing a multiple implantation to produce the temporarily effective area.

Claim 59 (Previously presented). The method as claimed in claim 53, further comprising performing the implantation through a metal foil.

Claim 60 (Previously presented). The method as claimed in claim 53, further comprising performing an implantation with protons to produce a steady-state field stopping area.

Claim 61 (Previously presented). The method as claimed in claim 53, wherein the implantation is performed from a side opposite a side closest to the pn junction.

Claim 62 (Previously presented). A semiconductor component comprising:

at least two electrodes; and

a semiconductor body coupled to the at least two electrodes, the semiconductor body including at least one pn junction and a voltage taking-up region of a first conduction type in which a space charge zone propagates if a voltage that reverse-biases the pn junction is applied to the electrodes,

wherein the voltage taking-up region further includes a temporarily effective area of the first conduction type having, between a conduction band and a valence band, centers

configured to trap free charge carriers in the event of flooding of the voltage taking-up region, and to discharge the charge carriers in the event of propagation of the space charge zone, wherein the temporarily effective area is arranged at a depth of substantially between 0.75 w_B to 0.95 w_B from the pn junction, where w_B denotes the distance between the pn junction and an opposite edge of the voltage taking-up region.